

# ABSTRACT

0060445-404900  
The present invention is a self-test circuit(BIST)  
incorporated in the memory device, which is activated in  
response to a test activation signal from outside. When  
5 this self-test circuit is activated in response to a test  
activation signal(WBIZ) from outside, it generates a test  
operation command(WBI-CMD), generates a test  
address(WBI-ADD), and generates test data(WBI-DATA).  
Furthermore, after the self-test circuit writes the test  
10 data to a memory cell, it effects a comparison to establish  
whether or not the read data that is read from this memory  
cell is the same as the test data that was written thereto  
and stores information as to the result of this comparison.  
This comparison result information is then output to the  
15 outside.